holes in the thickness direction in a tape substrate having an area able to accommodate a plurality of semiconductor package units and provided at its bottom surface with a metal interconnection layer and a solder resist layer and forming throughholes in the thickness direction in the solder resist layer; filling a conductive material in the through holes of the tape substrate in amounts incompletely filling the through holes; inserting connection terminals of a number of semiconductor elements required for forming a plurality of semiconductor package units into the corresponding through holes of the tape substrate and filling the gaps between the connection terminals and the inside walls of the through holes by the conductive material until about the top ends of the through holes; bonding and mounting semiconductor elements on the top surface of the tape substrate; forming a sealing resin layer covering the top surface of the tape substrate other than the regions where the semiconductor elements are mounted and sealing the area around the side surfaces of the semiconductor element; grinding and polishing to a predetermined thickness the top part of the sealing resin layer and the back surface portions of the semiconductor elements; and cutting the tape substrate into semiconductor package units to obtain individual semiconductor devices. By providing connection terminals extending downward from the active surface of the semiconductor element and inserted into the through holes of the tape substrate and a filler comprised of a conductive material filling the gap between the connection terminals and the inner walls of the through holes of the tape substrate and electrically connecting the connection terminals and metal interconnections, it is possible to directly bond the semiconductor element to the tape substrate at the active surface and possible to electrically connect the semiconductor element to the metal interconnection layer by the connection terminals inserted in the through holes of the tape substrate and the filler comprised of the

provided with conductor columns passing through the frame and the tape substrate at a region where the frame is formed, having top ends exposed at the top surface of the frame, and having bottom ends electrically connected to the metal interconnection layer. These preferred structures are particularly advantageous when applied to a multilayer semiconductor device. A multilayer semiconductor device produced in this way is comprised of a plurality of such semiconductor devices stacked in layers, wherein the semiconductor devices of each layer are connected with each other at the top ends of the conductor columns and the bottom ends of the external connection terminals. Preferably, the connection terminals extending downward from the active surface of the semiconductor element are bumps comprised of gold or copper. Preferably, the external connection terminals filling and passing through the openings of the solder resist layer are arranged in a peripheral or area array mode according to the application of the semiconductor device or the requirements of the customer. Preferably, the filler is filled in the gaps between the connection terminals and the through holes of the tape substrate up to positions of substantially the top ends of the through holes. That is, the amount of the filler is set so that the total volume with the connection terminals of the semiconductor element inserted later becomes substantially equal to the volume of the through holes of the tape substrate (with bottom portions defined by the metal interconnections). Due to this, the connection terminals and metal interconnections are reliably connected and, simultaneously, overflow of excess conductive material from the top ends of the through holes is prevented. As the conductive material, use may be made of a low melting point metal or a conductive paste. Preferably, since the heights of the large number of

Eighth Embodiment

Figure 29 shows, in sectional views, an example of a semiconductor device according to the seventh aspect of the present invention. The semiconductor device 104 shown in Fig. 29(1) is comprised of a resin member 124 of a predetermined thickness in which a semiconductor element 123 is sealed. The semiconductor element 123 has a back surface 123B exposed at the top surface of the resin member 124 and has an active surface 123A facing downward. Metal interconnections 125 are formed at the bottom surface of the resin member 124. Connection terminals 129 extending downward from the active surface 123A of the semiconductor element 123 are connected to the top surfaces of the metal interconnections 125. The top surface of the resin member 124 and the back surface 123B of the semiconductor element 123 form the same plane. The connection terminals 129 are formed as gold stud bumps, plated bumps, etc. The semiconductor device 104' shown in Fig. 29(2) is structured the same as the semiconductor device 104 of Fig. 29(1) except that the bottom surface of the resin member, including the metal interconnections 125, is covered by a solder resist layer 126 and that connection bumps 128 formed on the bottom surfaces of the metal interconnections 125 pass through the solder resist layer 126 and project downward. Referring to Fig. 30, an explanation will be given of the process of production of the semiconductor devices 104 and 104' shown in Fig. 29. The present embodiment can be applied to the case of producing a large number of semiconductor package units all together in the same way as in the first to fourth embodiments, but for simplification of the explanation, an explanation will be made of a single semiconductor package unit. First, as shown in Fig. 30(1), the semiconductor element 123 is mounted on a metal substrate 125M by bonding the front ends of the connection terminals 129